# High Dynamic Range Imaging with High Speed MSB Subframe Readout of In-Pixel Counters in SPAD Image Sensors

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***Abstract*—We propose a high dynamic range (HDR) imaging method using the most significant bit (MSB) subframe readout to extend the dynamic range (DR) without increasing the in-pixel counter bit depth. In this method, binary MSB images are generated at high speed during exposure, and a final image is obtained by combining these subframes with the multi-level image captured after exposure. The chip is fabricated using a 0.18 µm CMOS process and features a 64×32 SPAD pixel array with a 7-bit in-pixel counter. Experimental results show that the proposed approach enhances the photon detection capability while maintaining measurement accuracy.**

## I. INTRODUCTION

Single-photon avalanche diode (SPAD)-based image sensors are being developed as a promising technology for both low dark noise and high dynamic range (HDR) imaging. They have been widely studied in various fields, including security, automotive applications, and bioimaging. In particular, the demand for HDR imaging has been increasing in recent years, making the development of HDR imaging techniques with SPAD image sensors a crucial research topic. In HDR imaging with SPAD sensors, expanding the bit depth of the in-pixel counter increases dynamic range (DR) but also leads to a larger circuit area, which reduces spatial resolution. Consequently, there is a trade-off between DR extension and spatial resolution [1,2].

To address this trade-off, it is necessary to develop a photon counting algorithm that enables the detection of a larger number of photons while maintaining a low in-pixel counter bit depth. In response, we propose a photon counting method using the most significant bit (MSB) subframe readout as a different approach to achieving HDR imaging without requiring a higher in-pixel counter bit depth. This method sequentially reads out only the MSB for each subframe and combines multiple temporally divided data to achieve an effectively higher bit depth.

## II. PROPOSED ARCHITECTURE

Figure 1 shows the proposed architecture. To realize HDR imaging while suppressing the bit-depth of the in-pixel counter, we propose an imaging method utilizing subframes, distinct from the previous works [2-5]. In this approach, a binary image representing the MSB of the $N$-bit in-pixel counter is generated as a subframe at high speed during the exposure period. Furthermore, after the exposure is complete, an $N$-bit image is generated using the values of all bits of the in-pixel counter. Finally, the subframe binary images obtained during the imaging period, along with the multi-level image captured after exposure, are processed to generate a final image corresponding to the entire imaging period.

As illustrated in Fig. 2, when the photon count exceeds $2^{N-1}$ in an $N$-bit counter, a carry operation occurs at the MSB. To compute the total number of detected photons, the number of pixels with a "1" value in the binary output image is multiplied by $2^{N-1}$, and the final N-bit counter value is added to this product.

In this method, when outputting a subframe binary image, only the MSB of the in-pixel counter is reset. This operation ensures that the lower bits of the counter remain unchanged even after the MSB reset, allowing for continuous photon counting over time. To further extend the DR, the exposure control is applied through sub-sampling to reduce the number of photon detection pulses. This helps prevent the in-pixel counter from saturating during the subframe imaging period.

## III. IMPLEMENTATION

The chip block diagram and micrograph with the MSB subframe architecture are presented in Fig. 3. The chip is fabricated using a standard 0.18 µm CMOS process, and the SPAD pixel array comprises 64×32 pixels. The MSB is read out in parallel from eight pixels, allowing high-speed subframe readout. The overall configuration of the pixel circuit, its layout, and the pixel micrograph are shown in Figs. 4, 5, and 6, respectively. The in-pixel counter has a 7-bit depth, and an exposure control circuit is placed before the digital counter so that photon detection pulses can be reduced under high-light conditions when necessary. A current-controlled passive quenching circuit, commonly used for HDR imaging, is also employed [6, 7]. The pixel layout description and cross-sectional view are shown in Fig. 7.

A summary of the specifications is provided in Table I. In addition, to mitigate the paralyzing effect and lower power consumption, a clocked recharge method is adopted. The clock period is set to 1 µs to prevent the in-pixel counter from saturating during the subframe imaging period.

## IV. RESULTS

### A. Pixel Characteristics

The doping concentrations and electric field intensity distribution at the breakdown voltage, obtained through TCAD simulations, are shown in Fig. 8. Figure 9 presents both the TCAD simulation and experimental results of the I-V curves. The measured breakdown voltage was 8.4 V.

The breakdown voltage variation versus temperature is shown in Fig. 10. It indicates a temperature coefficient of 5.49 mV/K.

In our SPAD, the cathode voltage ($V_{\mathrm{cathode}}$), applied through the quenching transistor, and the anode voltage ($V_{\mathrm{anode}}$), directly applied to the SPAD, have different influences on the dark count rate (DCR). Figure 11 presents the relationship between the effective excess bias ($V_{\mathrm{ex}}$) and the DCR when $V_{\mathrm{anode}}$ is fixed at 7.1 V and $V_{\mathrm{cathode}}$ is varied. In contrast, Fig. 12 illustrates the variation in the DCR when $V_{\mathrm{cathode}}$ is fixed, and $V_{\mathrm{anode}}$ is changed. We believe these differences are partly due to the concentration of the electric field near the anode, as well as the direct contact between the $p^+$ region and the shallow trench isolation (STI).

Figure 13 shows the relationship between temperature and DCR. The results indicate that the increase in DCR is relatively small even with temperature fluctuations. Therefore, based on the findings in Figs. 10 and 13, temperature variations have a greater impact on the breakdown voltage than on the DCR. This suggests that to effectively suppress DCR, a bias voltage adjustment mechanism that compensates for temperature changes needs to be developed.

### B. Experimental Validation of the MSB Subframe Readout

Figure 14 shows the relationship between incident light intensity and the number of detected photons when the proposed MSB subframe readout method is employed. In this evaluation, 255 subframes were used within a single exposure duration without any exposure control. The findings demonstrate that while a 7-bit in-pixel counter alone limits the photon count to a maximum of 127, the proposed approach extends the detectable photon count to 16,447. This corresponds to the photon detection capability of a 14-bit in-pixel counter, theoretically leading to a DR expansion of approximately 42 dB. These results verify that leveraging MSB subframes alleviates the constraints imposed by the counter bit-depth, thereby enabling more efficient photon detection. Moreover, the linearity of the obtained curve substantiates that the accuracy of photon counting remains uncompromised even with the proposed approach. Increasing the number of subframes further enhances the photon detection capability.

Figure 14 also presents the measurement results when the paralyzing effect is exploited. As shown in Fig. 12, DCR of the SPAD became extremely large at $V_{\mathrm{anode}}$ = 8.8 V and $V_{\mathrm{cathode}}$ = 3.0 V. Under this high-DCR condition, if incident light is applied without clocked recharge, the photon detection count decreases proportionally to the light intensity due to the paralyzing effect. This demonstrates that by inverting the output count in an external circuit, a linear response to light intensity can be obtained. Furthermore, compared to conventional clocked recharge operation, this approach enables a linear response over a wider illumination range by ensuring sufficient bias voltage application.

Figure 15 indicates the imaging results with and without the proposed MSB subframe technique under identical exposure conditions at $V_{\mathrm{ex}}$=0.8 V. The results validate that the proposed method effectively prevents saturation in high-illumination regions, thereby contributing to an extended DR. Figure 15 also includes an image captured using the paralyzing effect. While our SPAD requires sufficiently high bias voltage to function properly, increasing the bias voltage also exacerbates the impact of DCR. If a low DCR device were used, an image obtained by the paralyzing effect could be acquired.

## V. CONCLUSION

In this study, we implemented a photon counting method utilizing high-speed MSB subframe readout of the in-pixel counter and demonstrated its effectiveness.


## ACKNOWLEDGMENT

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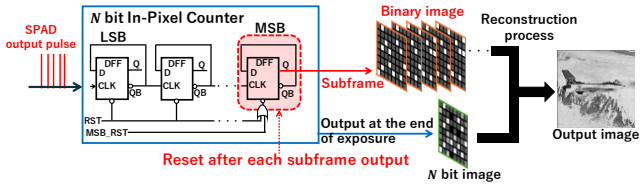



**Figure 1.** Proposed MSB subframe architecture.

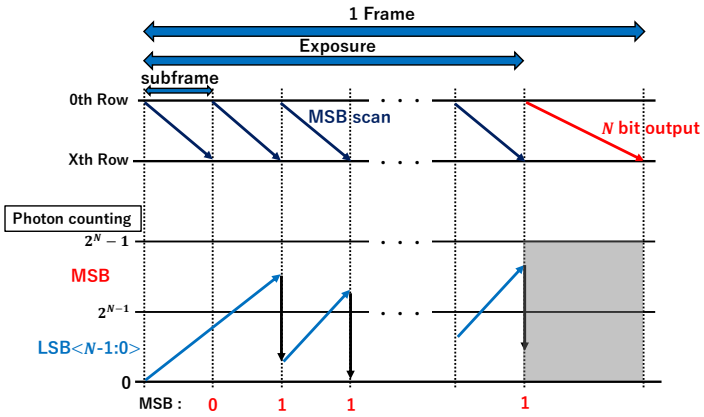
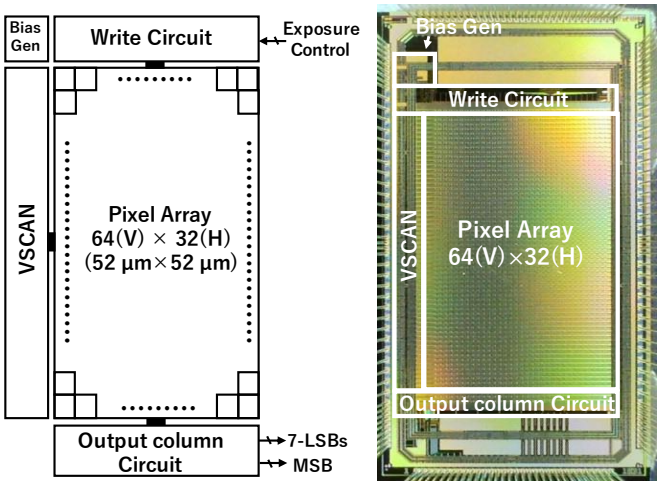



**Figure 2.** Concept of MSB subframe readout and in-pixel counter value.




(a) (b)

**Figure 3.** Chip (a) block diagram, (b) micrograph.

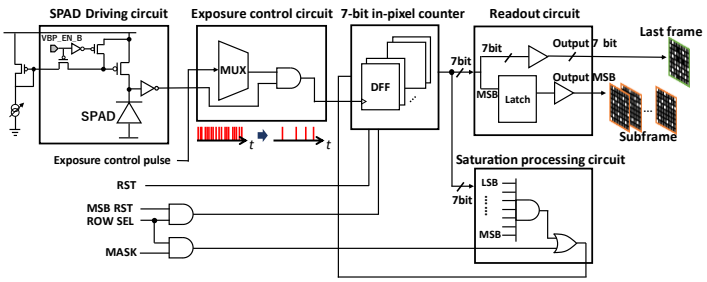



**Figure 4.** Overall pixel circuit configuration.

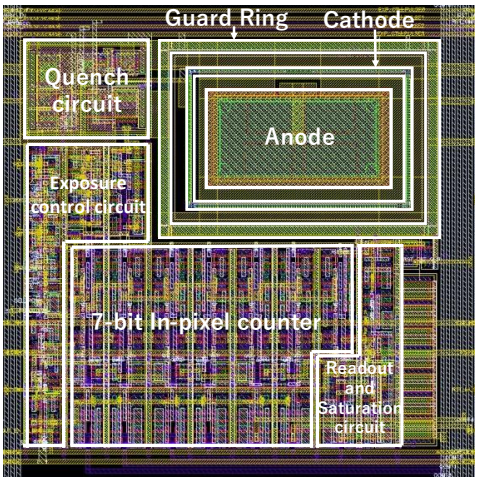



**Figure 5.** Layout of the pixel circuit.

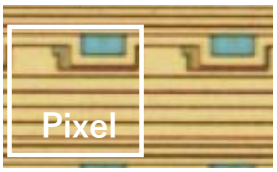



**Figure 6.** Pixel micrograph.

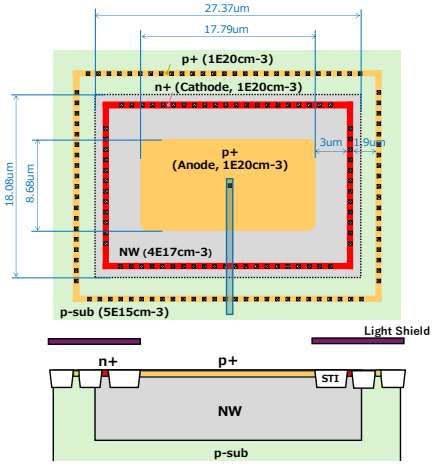



**Figure 7.** Layout description of the single SPAD. Below is a cross-sectional view of the SPAD.

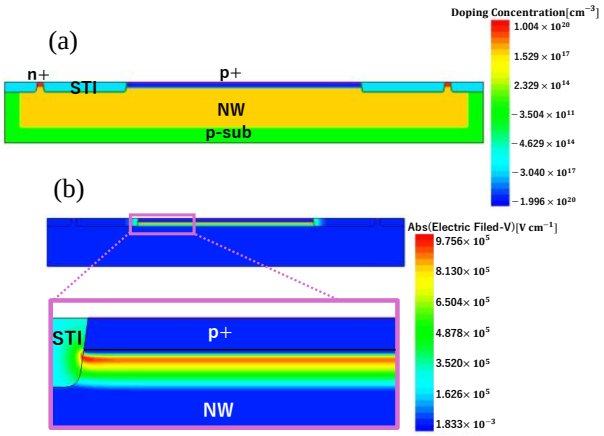



**Figure 8.** TCAD simulation results of SPAD. (a) Doping concentration. (b) Electric field.

**Table I.** Chip characteristics.

| | |
|---|---|
| **Process** | 0.18μm 1P5M Standard CMOS |
| **Power Supplies** | 1.8 V, 3.3 V, 5.0 V, -9.0 V |
| **Die Size** | 2.52 mm × 5.18 mm |
| **Number of Pixels** | 64 (V) × 32 (H) |
| **Pixel Size** | 52 μm × 52 μm |
| **Fill Factor** | 5.8% |
| **In-pixel Counter** | 7-bit |
| **Exposure Time** | 32.64 ms |
| **Subframe Period** | 128 μs |
| **Number of Subframes** | 255 |
| **Frame Rate** | 30 fps |
| **Breakdown Voltage** | 8.4 V |
| **Dark Count Rate** | Typ. 17.3 cps/μm² ($@V_{ex}$ = 800 mV, room temp.) |

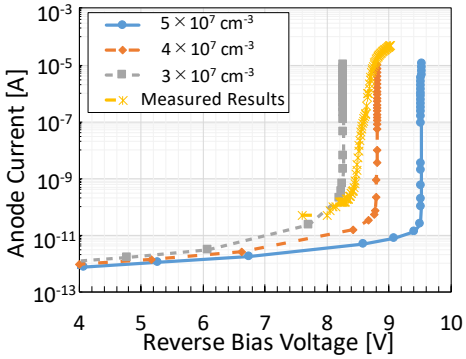



**Figure 9.** Static SPAD current as a function of the reverse bias voltage (*I-V* curve).

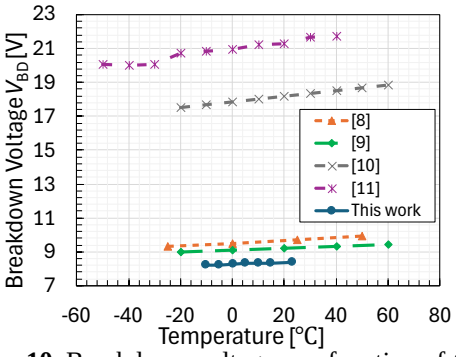



**Figure 10.** Breakdown voltage as a function of temperature.

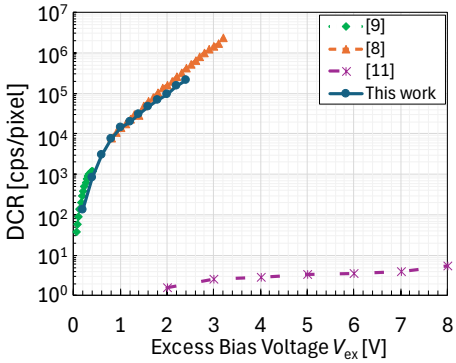



**Figure 11.** DCR as a function of excess bias voltage.

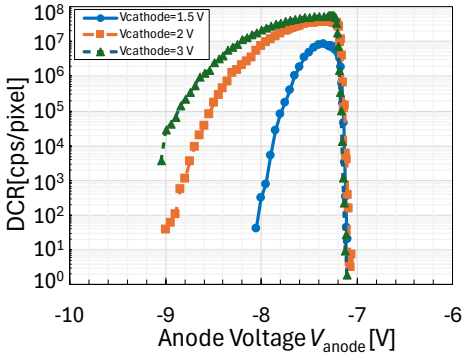



**Figure 12.** Relationship between anode voltage and DCR.

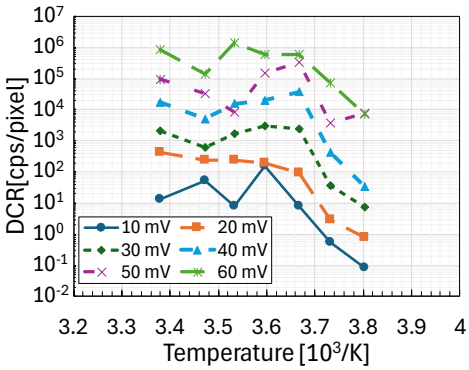



**Figure 13.** DCR as a function of the inverse of temperature for different excess bias voltages.

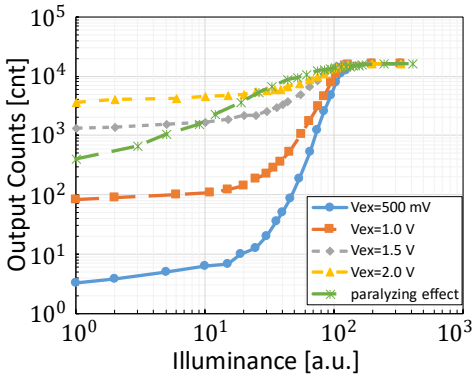
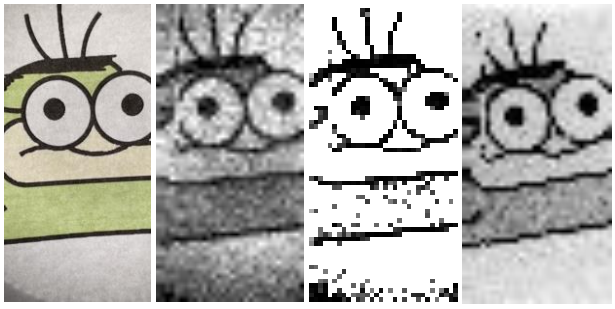



**Figure 14.** Reconstructed output pixel counts as a function of incident illuminance at 30 fps.



(a) (b) (c) (d)

**Figure 15.** Output images.
(a) Reference image.
(b) Imaging results using the proposed method.
(c) Imaging results using in-pixel counter only.
(d) Imaging results using paralyzing effect.